

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 212005US2		SERIAL NO. NEW APPLICATION	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Hans Jurgen MATTAUSCH, et al.			
				FILING DATE HEREWITH		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
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	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
PmV	AO	2000-276400	10/6/00	JAPAN			X
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
PmV	AW	H. J. MATTAUSCH, "HIERARCHICAL ARCHITECTURE FOR AREA-EFFICIENT INTEGRATED N-PORT MEMORIES WITH LATENCY-FREE MULTI-GIGABIT PER SECOND ACCESS BANDWIDTH", ELECTRONICS LETTERS, August 19, 1999, Vol. 35, No. 17, pages 1-2					
	AX						
	AY						
	AZ						
Examiner <i>burn w. Deal</i>					Date Considered <i>7/21/03</i>		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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 08/02/01

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 212005US2		SERIAL NO. 09/919,859	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Han Jurgen MATTAUSCH et al.			
				FILING DATE 08/02/01		GROUP 2185	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		PATENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
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FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
PMV	AO	2000-276400	10/06/00	JAPAN (corresponds to U.S. Serial Number 09/533,336, filed March 23, 2000)			X
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
PMV	AW	H. J. MATTAUSCH, "HIERARCHICAL ARCHITECTURE FOR AREA-EFFICIENT INTEGRATED N-PORT MEMORIES WITH LATENCY-FREE MULTI-GIGABIT PER SECOND ACCESS BANDWIDTH", ELECTRONICS LETTERS, August 19, 1999, Vol. 35, No.17, pages 1-2					
	AX						
	AY						
	AZ						
Examiner <i>David M. Pate</i>					Date Considered <i>7/21/03</i>		

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